Amendments to the Specification

Please replace the paragraph beginning on page 2, line 1 with the following amended paragraph:

As shown in Fig. 6a, the SOI wafer 12 includes a buried oxide (referred to as "BOX" hereinafter) layer 16 stacked on a semiconductor substrate 14 and a semiconductor layer 18. To begin with, a field oxide film 20 is formed on the semiconductor layer 18, thereby insulating the semiconductor layer 18 with the BOX layer 16 and the field oxide film 20. Then, as shown in Fig. 6b, a gate oxide film 22 is formed on the semiconductor layer 18. Furthermore, as shown in Fig. 6c, channel ions of a medium dose amount are implanted in the interface between the semiconductor layer 18 and the gate oxide film 22. Still further, as shown in Fig. 6d, a source/drain region [[20]] 28 is formed in the semiconductor layer 18 after forming a gate electrode 26 on the gate oxide film 22. Finally, an FET of the MOS type (referred to as "MOSFET" hereinafter) is completed by forming a inter-layer insulating film 30, contact holes 32, buried plugs 34, and a wiring layer 36. In the MOSFET formed on the SOI wafer 12, the channel region and the source/drain region 28 are formed on the BOX layer 16. Therefore, an LSI of the low power consumption type can be achieved without forming any depletion layer in the semiconductor substrate 14.

Please replace the paragraph beginning on page 13, line 11 with the following amended paragraph:

Similar to the above, the conductive layers 102 made of Au, Pt, and Al have a resistivity of 2.4 x $10^{-6}\Omega\cdot$ cm, 10.6 x $10^{-6}\Omega\cdot$ cm, and 2.75 x $10^{-6}\Omega\cdot$ cm, respectively. Now, again let us consider the resistance of the conductive layer 102 by letting the film thickness of the conductive layer 102 be 10nm and assuming a rectangle shaped region of the conductive layer 102. If the region has a width of 1cm and a length equal to the distance from the center of the SOI wafer 12 with a diameter of 150mmφ to the edge of the same i.e. 75mm, an Au layer, a Pt layer, and an Al layer as the conductive layer 102 have a resistance of 180Ω, 794Ω, and 206Ω, respectively. If B+ 24 is implanted against the conductive layer 102 at the dose amount of ~~1 x 1013 ions/cm2~~ 1 x 10^{13} ions/cm2 for one minute, the ion current becomes 27nA/cm2, the charge-up potential difference of the semiconductor layer 18 becomes no more than 5mV in the Au layer, 0.02mV in the Pt layer, and 6mV in the Al layer, respectively. Still further, the FN current flowing through the gate oxide film 22 is 1.3 x 10^{-5}A(13μA)/cm2 at the potential difference of 6V to 8V if the thickness of the gate oxide film 22 is in the range of 6nm to 8nm. Therefore, if the above-mentioned metal materials are adopted for forming the conductive layer 108, the potential difference due to the electrical charge 38 charged up in the semiconductor layer 18 can not exceed 10V. However, in case of adopting the above-mentioned metal materials for forming the conductive layer 102, it is preferable

that the conductive layer is formed so as to have a thickness of less than 5nm.

Please replace the paragraph beginning on page 14, line 4 with the following amended paragraph:

Furthermore, if Al is adopted to form the conductive layer 102, Al can function as acceptors for ~~elections~~ electrons in the semiconductor layer 18 made of Si. Therefore, even though the ion ~~plantation~~ implantation of B+ 24 is executed in the knock-on state, there is no generation of the recombination center accompanied by impurities and lattice defects of the semiconductor layer 18, thus nothing deteriorating the characteristics of the FET element being caused.

Please replace the paragraph beginning on page 16, line 12 with the following amended paragraph:

Next, another method for manufacturing a semiconductor device 200 according to the second embodiment of the invention will be described with reference to ~~Figs. 3~~ Figs. 3a – 3e and 4. This embodiment is characterized in that the conductive layer 102 is formed before forming the gate oxide layer 22. Figs. 3a through 3e are schematic cross-sectional illustrations for describing the steps of another method for manufacturing a semiconductor device 200 according to the invention, and Fig. 4 is a schematic cross-sectional illustration for describing the state of the semiconductor device 200 at the time of the ion implantation as shown in Fig. 3b.